CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A multilayer dielectric tunnel barrier structure for use in semiconductor memory devices, said tunnel barrier structure comprising:

   a substrate supporting a magnetic layer;

   an ALD deposited first nitride junction layer formed over said magnetic layer;

   an ALD deposited intermediate junction layer formed over said first nitride junction layer; and

   an ALD deposited second nitride junction layer formed over said intermediate tunnel junction layer.

2. A structure as in claim 1, wherein said magnetic layer is a ferromagnetic layer.

3. A structure as in claim 2, wherein said ferromagnetic layer is pinned.

4. A structure as in claim 2, wherein said ferromagnetic layer is free.

5. A structure as in claim 1, wherein said first nitride junction layer is formed of one or more nitride monolayers.

6. A structure as in claim 5, wherein said first nitride junction layer is formed of AlN.

7. A structure as in claim 6, wherein said first nitride junction layer has a thickness of approximately .8 A° to approximately 58 A°.

8. A structure as in claim 1, wherein said intermediate junction layer is an oxide layer.

9. A structure as in claim 8, wherein said oxide layer is formed of one or more monolayers.

10. A structure as in claim 9, wherein said oxide layer is formed of Al_xO_y, HfO, Ta_2O_5, SiO_2, or combinations thereof.

11. A structure as in claim 1, wherein said intermediate junction layer is formed on said first nitride junction layer

12. A structure as in claim 11, wherein said intermediate junction layer and first nitride junction layer is approximately 1.6 A° to approximately 59 A° thick.

13. A structure as in claim 12, wherein said intermediate junction layer has a thickness of approximately .8 A° to approximately 58 A°.

14. A structure as in claim 1, wherein said second nitride junction layer is formed from one or more nitride monolayers.

15. A structure as in claim 14, wherein said second nitride junction layer is formed of AlN.

16. A structure as in claim 1, wherein said second nitride junction layer and intermediate junction layer and first nitride junction layer is approximately 2.4 A° to approximately 60 A° thick.

17. A structure as in claim 16, wherein said second nitride junction layer has a thickness of approximately .8 A° to approximately 58 A°.

18. A structure as in claim 16, wherein said second nitride junction layer interfaces with a ferromagnetic layer.

19. A structure as in claim 18, wherein said ferromagnetic layer is pinned.

20. A structure as in claim 18, wherein said ferromagnetic layer is free.

21. A structure as in claim 1, wherein said first and second nitride junction layers are approximately 4 A° thick and the intermediate junction layer is approximately 4 A° thick.

22. A structure as in claim 1, wherein said first and second nitride junction layers are approximately 2 A° thick and the intermediate junction layer is approximately 6 A° thick.

23. A structure as in claim 1, wherein said first and second nitride junction layers are approximately 4 A° thick and the intermediate junction layer is approximately 10 A° thick.

24. A structure as in claim 1, wherein said first and second nitride junction layers are approximately 20 A° thick and the intermediate junction layer is approximately 40 A° thick.

25. A method of fabricating a multilayer dielectric tunnel barrier structure for use in semiconductor memory devices, said method comprising:

providing a substrate supporting a magnetic layer;

forming an ALD deposited first nitride junction layer over said magnetic layer;

forming an ALD deposited intermediate junction layer over said first nitride junction layer; and

forming an ALD deposited second nitride junction layer over said intermediate tunnel junction layer.

26. The method as in claim 25, wherein said magnetic layer is a ferromagnetic layer.

27. The method as in claim 26, wherein said ferromagnetic layer is pinned.

28. The method as in claim 26, wherein said ferromagnetic layer is free.

29. The method as in claim 25, wherein said first nitride junction layer is formed of one or more nitride monolayers.

30. The method as in claim 29, wherein said first nitride junction layer is formed of AlN.

31. The method as in claim 30, wherein said first nitride junction layer is formed in a reaction vessel with heated gas lines.

32. The method as in claim 31, wherein said gas lines are heated from a temperature of approximately 40°C to approximately 120°C.

33. The method as in claim 31, wherein said heated gas lines introduce a first reactant into the reaction vessel.

34. The method as in claim 33, wherein said first reactant is TMA.

35. The method as in claim 33, wherein said first reactant is NH_3.

36. The method as in claim 33, wherein said first reactant is purged.

37. The method as in claim 36, wherein a second reactant is carried through a heated gas line into the reaction vessel.

38. The method as is claim 37, wherein said second reactant is TMA.

39. The method as in claim 37, wherein said second reactant is NH_3.

40. The method as in claim 37, wherein said second reactant is purged.

41. The method as in claim 40, wherein said one or more first nitride junction layers of AlN are formed.

42. The method as in claim 41, wherein said first nitride junction layer is approximately .8 A° to approximately 58 A° thick.

43. The method as in claim 42, wherein said first nitride junction layer is thermally annealed.

44. The method as in claim 42, wherein said first nitride junction layer is not thermally annealed.

45. The method as in claim 25, wherein said intermediate junction layer is an oxide layer.

46. The method as in claim 45, wherein said oxide layer is formed of one or more oxide monolayers.

47. The method as in claim 46, wherein said oxide layer is formed of Al_xO_y, HfO, Ta_2O_5, SiO_2, or combinations thereof .

48. The method as in claim 47, wherein said oxide layer is formed in a reaction vessel with heated gas lines.

49. The method as in claim 48, wherein said gas lines are heated from a temperature of approximately 40°C to approximately 120°C.

50. The method as in claim 48, wherein said heated gas lines introduce a first reactant into the reaction vessel.

51. The method as in claim 50, wherein said first reactant is TMA.

52. The method as in claim 50, wherein said first reactant is H_2O.

53. The method as in claim 50, wherein said first reactant is purged.

54. The method as in claim 53, wherein a second reactant is carried through a heated gas line into the reaction vessel.

55. The method as is claim 54, wherein said second reactant is TMA.

56. The method as in claim 54, wherein said second reactant is H_2O.

57. The method as in claim 54, wherein said second reactant is purged.

58. The method as in claim 57, wherein said one or more intermediate junction layers of Al_xO_y is formed.

59. The method as in claim 58, wherein said intermediate junction layer is formed on said first nitride junction layer

60. The method as in claim 59, wherein said intermediate junction layer and first nitride junction layer is approximately 1.6 A° to approximately 59 A° thick.

61. The method as in claim 60, wherein said intermediate junction layer has a thickness of approximately .8 A° to approximately 58 A°.

62. The method as in claim 61, wherein said intermediate junction layer is thermally annealed.

63. The method as in claim 61, wherein said intermediate junction layer is not thermally annealed.

64. The method as in claim 25, wherein said second nitride junction layer is formed of one or more nitride monolayers.

65. The method as in claim 64, wherein said second nitride junction layer is formed of AlN.

66. The method as in claim 65, wherein said second nitride junction layer is formed in a reaction vessel with heated gas lines.

67. The method as in claim 66, wherein said gas lines are heated from a temperature of approximately 40°C to approximately 120°C.

68. The method as in claim 66, wherein said heated gas lines introduce a first reactant into the reaction vessel.

69. The method as in claim 68, wherein said first reactant is TMA.

70. The method as in claim 68, wherein said first reactant is NH_3.

71. The method as in claim 68, wherein said first reactant is purged.

72. The method as in claim 71, wherein a second reactant is carried through a heated gas line into the reaction vessel.

73. The method as is claim 72, wherein said second reactant is TMA.

74. The method as in claim 72, wherein said second reactant is NH_3.

75. The method as in claim 72, wherein said second reactant is purged.

76. The method as in claim 75, wherein said one or more second nitride junction layers of AlN is formed.

77. The method as in claim 25, wherein said second nitride junction layer and intermediate junction layer and first nitride junction layer is approximately 2.4 A° to approximately 60 A° thick.

78. The method as in claim 77, wherein said second nitride junction layer has a thickness of approximately .8 A° to approximately 58 A°.

79. The method as in claim 78, wherein said second nitride junction layer undergoes a nitrogen plasma anneal.

80. The method as in claim 78, wherein said second nitride junction layer does not undergo a nitrogen plasma anneal.

81. The method as in claim 78, wherein said second nitride junction layer interfaces with a ferromagnetic layer.

82. The method as in claim 81, wherein said ferromagnetic layer is pinned.

83. The method as in claim 81, wherein said ferromagnetic layer is free.

84. A system comprising:

a processor; and

a memory device coupled to said processor, at least one of said processor and said memory device using a magnetic tunnel junction structure; at least one of said processor and said memory device and said magnetic tunnel junction structure comprising a multilayer dielectric tunnel barrier structure, said tunnel barrier structure comprising:

a substrate supporting a magnetic layer;

an ALD deposited first nitride junction layer formed over said magnetic layer;

an ALD deposited intermediate junction layer formed over said first nitride junction layer; and

an ALD deposited second nitride junction layer formed over said intermediate tunnel junction layer.

85. A system as in claim 84, wherein said magnetic layer is a ferromagnetic layer.

86. A system as in claim 85, wherein said ferromagnetic layer is pinned.

87. A system as in claim 85, wherein said ferromagnetic layer is free.

88. A system as in claim 84, wherein said first nitride junction layer is formed of one or more nitride monolayers.

89. A system as in claim 88, wherein said first nitride junction layer is formed of AlN.

90. A system as in claim 89, wherein said first nitride junction layer has a thickness of approximately .8 A° to approximately 58 A°.

91. A system as in claim 84, wherein said intermediate junction layer is an oxide layer.

92. A system as in claim 91, wherein said oxide layer is formed of one or more oxide monolayers.

93. A system as in claim 92, wherein said oxide layer is formed of Al_xO_y, HfO, Ta_2O_5, SiO_2, or combinations thereof.

94. A system as in claim 91, wherein said intermediate junction layer is formed on said first nitride junction layer

95. A system as in claim 94, wherein said intermediate junction layer and first nitride junction layer is approximately 1.6 A° to approximately 59 A° thick.

96. A system as in claim 95, wherein said intermediate junction layer has a thickness of approximately .8 A° to approximately 58 A°.

97. A system as in claim 84, wherein said second nitride junction layer is formed of one or more nitride monolayers.

98. A system as in claim 97, wherein said second nitride junction layer is formed of AlN.

99. A system as in claim 84, wherein said second nitride junction layer and intermediate junction layer and first nitride junction layer is approximately 2.4 A° to approximately 60 A° thick.

100. A system as in claim 99, wherein said second nitride junction layer has a thickness of approximately .8 A° to approximately 58 A°.

101. A system as in claim 100, wherein said second nitride junction layer interfaces with a ferromagnetic layer.

102. A system as in claim 101, wherein said ferromagnetic layer is pinned.

103. A system as in claim 101, wherein said ferromagnetic layer is free.